

IN THE UNITED STATES PATENT OFFICE

Applicants: Eric R. Keller, et al.
Assignee: Xilinx, Inc.
Title: "Using Redundant Routing to Reduce Susceptibility to Single Event Upsets in PLD Designs"
Serial No.: 10/603,734 Filing Date: 6/24/2003
Examiner: Naum B. Levin Art Unit: 2825
Docket No.: X-1281 US Conf. No.: 3289

Mail Stop AF
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL CONFERENCE BRIEF

Dear Sir:

This Brief is submitted for the Pre-appeal Conference requested in the Notice of Appeal with which this Brief is submitted.

Grounds of Rejection

A. Claims 1-17 and 22-31 stand rejected under 35 USC §102(e) as being unpatentable over "Bauer" (US Patent No. 6,671,202).

B. Claims 18-21 are withdrawn as a result of a previous restriction.

Argument

A. The rejection of Claims 1-17 and 22-31 under 35 U.S.C. §102(e) should be withdrawn, because the claims clearly distinguish over Bauer.

Firstly, the rejection is traversed on the grounds that the claimed methods, media, and systems are clearly incompatible with the structures described by Bauer. In other words, the claimed methods cannot be practiced on Bauer's structures. Secondly, even if Bauer did in fact illustrate one or more structures on which the methods of the invention could be practiced (which Applicants do not concede), Bauer

in fact neither teaches nor suggests applying the claimed methods to these or any other structures.

In Applicants' claimed methods, during implementation of a design in the PLD, a single node ("the node") is routed on two different paths through the same multiplexer ("the programmable routing multiplexer"), using two different data input terminals of the multiplexer ("the first and second data input terminals"). A selection between the two input paths is controlled solely by a value stored in a single memory cell controlling the multiplexer ("the first memory cell"), and thus potentially subject to single event upset (SEU). However, because the selection is controlled solely by the contents of the one memory cell, such an SEU will merely change the selection from one of the paths to the other (e.g., from the first routing path to the second routing path, or *vice versa*), and they each provide the same input signal to the multiplexer on a different data input terminal. Thus, an SEU that incorrectly changes the select function of the multiplexer by changing the value stored in the select memory cell still leaves the multiplexer providing the correct output signal.

Bauer's Fig. 1 shows a structure in which there are no two input paths between which a selection is controlled solely by a value stored in a single memory cell. Each input path is controlled by a separate memory cell. Therefore, Fig. 1 does not illustrate a multiplexer in which "a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer".

Bauer's Figs. 4 and 5 show structures in which at most one memory cell can have an enable value at any given time (see Bauer's abstract and Figs. 4 and 5). Thus, if a first pass gate is enabled by a value stored in a first memory cell, selecting a first path through the multiplexer, a second pass gate selecting a second path is necessarily disabled. If a single event upset (SEU) occurs in any of the disabling memory cells, the value stored in the memory cell does not change, and the associated paths remain disabled. If an SEU occurs in the enabling memory cell, the path associated with that memory cell becomes disabled. (Abstract.) Therefore, it is not possible for a single event upset to change a selection from one path to another path, but at most to change a selection of one path to no selected path. Therefore,

these structures also fail to illustrate a multiplexer in which "a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer". Therefore, not only do these structures render it impossible to perform the claimed identification:

identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer (Claim 1)

but they also provide no motivation to route the node on two different routing paths as claimed:

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal; and routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.
(Claim 1)

because there is no advantage to doing so in Bauer's structures.

Therefore, Bauer neither teaches nor suggests a structure in which "a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer". Since it is not possible to find two such input paths, the claimed methods cannot be practiced on such a structure.

Each of Claims 1, 8, 10, 12, 22, 28, and 30 specifies that "a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer". Clearly, such a selection cannot be made using the structures of Bauer's Figs. 1, 4, and 5. Further, even if Bauer's figures did in fact illustrate a structure on which the methods of the invention could be practiced (which Applicants do not concede), Bauer in fact neither teaches nor suggests applying the claimed method steps. For example, Bauer neither teaches nor suggests routing the same node on both first and second routing paths through the routing multiplexer. Applicants are not claiming a multiplexer structure, but

methods, media, and systems for implementing a design in a multiplexer structure, and Bauer clearly neither teaches nor suggests these methods, media, or systems.

Therefore, and for at least these reasons, Claims 1, 8, 10, 12, 22, 28, and 30 distinguish over Bauer. Claims 2-7, 9, 11, 13-17, 23-27, 29, and 31 also distinguish over Bauer for at least the reasons of these claims, from which they respectively depend. Therefore, the rejection of Claims 1-17 and 22-31 should be reversed.

Applicants also respectfully note that the rejection of Claims 7, 9, 11, 17, 27, 29, and 31 included in the Office Actions have been inadequate, despite repeated requests that this inadequacy be addressed. These claims specify that the method/program/system further comprises evaluating the source and destination logic (or node) and determining that the source and destination logic (or node) do not form a portion of a triple modular redundancy (TMR) circuit. Bauer neither teaches nor suggests this feature of the claims. Hence, Claims 7, 9, 11, 17, 27, 29, and 31 further distinguish over Bauer for at least this additional reason. Therefore, and for at least these additional reasons, the rejection of Claims 7, 9, 11, 17, 27, 29, and 31 should be reversed.

Conclusion

In view of the above, Appellants submit that the rejections are improper, the claimed invention is patentable, and the rejections of Claims 1-17 and 22-31 should be reversed. Appellants respectfully request reversal of the rejections as applied to the appealed claims and allowance of the entire application.

*I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent & Trademark
Office on January 30, 2008.*

Pat Tompkins /Pat Tompkins/
Name Signature

Respectfully submitted,

/Lois D. Cartier/

Lois D. Cartier
Agent for Appellants
Reg. No. 40,941

Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)

Approved for use through xx/xx/200x. OMB 0651-00xx
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

X-1281 US

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on January 30, 2008

Signature /Pat Tompkins/

Typed or printed name Pat Tompkins

Application Number

10/603,734

Filed

06-24-2003

First Named Inventor

Eric R. Keller

Art Unit

2825

Examiner

Naum B. Levin

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☐ attorney or agent of record.
Registration number _____

☒ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 40,941

/Lois D. Cartier/ Reg. No. 40,941

Signature

Lois D. Cartier

Typed or printed name

720-652-3733

Telephone number

January 30, 2008

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.